Self-assembling semiconductor nanowires for device applications

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For the beyond-CMOS era, self-assembly is expected to play a major role, allowing further down-scaling, more ideal device performance, and still with reductions in fabrication costs. In this presentation I will give an update on the status of growth of 10nm-scale semiconductor nanowires based on a combination of top-down patterning and bottom-up growth and assembly of nanowires, including designed heterostructures for added functionalities. I will concentrate on III-V nanowires with a special interest in the ability to integrate such devices with Si-technology. I will, as example, primarily discuss wrapped insulator-gate field-effect transistors (WIGFETs), fabricated as dense arrays of epitaxially grown nanowire devices. Other examples or nanowire applications, such as for memories and opto-electronics, will also be described.
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